Abstract

A vertical signal processing circuit including a buffer and a polyphase filter, and adapted to simultaneously process vertical peaking and vertical scaling on pixel data in a first operational mode. In a first operational vertical peaking and scaling mode, the embodiment includes receiving pixel data at a first rate, circulating the data in line buffers and filtering the circulated data through a polyphase filter configured with coefficients derived by convolving peaking filter coefficients with scaling polyphase filter coefficients, and presenting processed pixel data for storage at a second, different pixel rate. Using a control circuit, the pixel-data processing circuit can switch between operational modes by setting different coefficients for the polyphase filter circuit.